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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,207	06/22/2001	Jonathan Schmitt	00-72 68605 (6653.)	8393

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Corporate Legal Department
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EXAMINER	
NGUYEN, DANNY	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,207	SCHMITT, JONATHAN	
	Examiner	Art Unit	
	Danny Nguyen	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-8, 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Agan (USPN 5,669,684).

Regarding to claim 1, Agan discloses a method for power protection circuit comprises the steps of placing the level shifter (10) in a pre-selected state (the power is applied to VR and transistors 16 and 18 are non-conductive, see fig. 1, col. 3, lines 45-47) if the input voltage supply (Vc) is not powered on before an output voltage supply (VR) is powered on (the power is applied to VR and transistors 16 and 18 are non-conductive, see fig. 1, col. 3, lines 45-47), and releasing the level shifter from the pre-selected state to follow transitions of an input signal when the input voltage supply and the output voltage supplies are powered on (see col. 3, lines 46-57 and col. 5, lines 24-27).

Regarding to claims 2 and 5, Agan discloses the step of connecting a common voltage rail to an output signal port (switch 20 grounds (common voltage) the output on line 24 (see fig. 1).

Regarding to claims 4 and 7, Agan discloses a power protection circuit comprises a latch (10, 30) coupled to an input supply (Vc) and output supply (col. 3, lines 3-4), and the latch sets a switch (e.g. switch 16)) connected to the latch (10, 30) to latch wherein the switch (16) has a first state for holding a level shifter (10) if the input voltage supply is not powered on before an output voltage supply is powered on (the power is applied to VR and transistors 16 and 18 are non-conductive, see fig. 1, col. 3, lines 45-47), and a second state for releasing the level shifter from the pre-selected state to follow transitions of an input signal when the input voltage supply is powered on (see col. 3, lines 46-57 and col. 5, lines 24-27).

Regarding claim 8, Agan discloses a switch (e.g. switch 16) connected to a level shifter (10 and 30) between an output signal port (port B) of the level shifter (10 and 30) an the ground (common voltage rail), an a latch (10) is connected to the switch to drive the switch (16) to conducting state when the input voltage (Vc) is not powered and when the output voltage is powered, to drive the switch to a non-conducting state if the input voltage and the output voltage are powered (The switch (20) goes to non-conducting state when there is power provided to the input whenever switch (16) is on).

Regarding claim 10, Agan discloses the latch (10) comprises a two-field effect transistor (32 and 34) connected in series between a third transistor (18) and common voltage (ground).

Regarding claims 3 and 6, Agan discloses the switch (16) presents high impedance (col. 3, lines 50-52) to the output port (port B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agan in view of Annema et al (USPN 6,320,414). Agan discloses a switch (16), but Agan does not disclose the switch comprises two transistors connected in series. Annema et al disclose switch (T1 and T2) coupled in series. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a switch of Agan as a switch with two transistors connected in series in order to improve current capacity.

Response to Arguments

3. Applicant's arguments filed 12/17/2003 have been fully considered but they are not persuasive.

Regarding amended claim 1, applicant argued that Agan does not disclose releasing the shifter (10) from the pre-selected state when the input voltage and the output voltage supplies are powered-on. Agan states that when power is applied at Vr (the output voltage supply Vr = 5.0 V) at a first time, and no power applied at Vc (the input voltage supply = 3.3 V), the level shifter (10) is held at off state since at this moment, the transistors (16 and 18) are non-conductive. As soon as, power is applied

at Vc at a second time, the input signal (38) will turn on the transistor (16), which cause point (A) and output (22) to be low. With node A low, the transistor (14) turn on and the level shifter (10) is released from the off state (e.g. see col 3, lines 3-10, and lines 45-55, and col. 5, lines 24-27). Thus, the shifter (10) is released from the pre-selected state (off-state) when the input and output voltage supplies are powered-on. Therefore, applicant's arguments of the amended claim 1 do not distinguish over Agan reference.

Regarding claim 4 applicant argued that Agan does not teach the latch sets the switch to a first state for holding the shifter in a pre-selected state and sets the switch to a second state for releasing the shifter from the pre-selected state when the input and output voltage supplies are powered-on. However, Agan discloses that the latch (10) sets the switch (e.g. switch 16) to a first state (the switch 16 is held at non-conductive state as the output voltage supply Vr is powered at a first time) and sets the switch (switch 16) to a second state (when both input and output voltage supplies are powered on, the switch 16 is set to a conductive state). Therefore, applicant's arguments of claims 4 do not over-come the Agan reference.

Regarding claim 8, applicant argued that Agan does not disclose the latch sets the switch is non-conducting state as the input and output voltage supplies are powered-on. However, Agan discloses in fig. 1 that as the input and output voltage supplies are powered-on, the control signal (38) will be high. With signal (38) high, the latch (10) sets the switch (18) is non-conducting state. Therefore, applicant's arguments of claim 8 do not distinguish over Agan reference.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (571)-272-2054. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)-272-2800X36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DN

DN
February 17, 2004

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800